晶采光電科技股份有限公司
AMPIRE CO., LTD

SPECIFICATIONS FOR LCD MODULE

CUSTOMER	
CUSTOMER PART NO.	
AMPIRE PART NO.	AM-240320LITZQW-01H
APPROVED BY	
DATE	

☐ Preliminary Specification
■ Formal Specification

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This Specification is subject to change without notice.

RECORD OF REVISION

Revision Date	Page	Contents	Editor
2022/08/03	-	New Release	Mantle

1. Features

LCD 2.4 inch Amorphous-TFT-LCD (Thin Film Transistor Liquid Crystal Display) for mobile-phone or handy electrical equipments.

(1) Construction: 2.4" a-Si color TFT-LCD, White LED Backlight and FPC.
(2) Main LCD : 2.1 Amorphous-TFT 2.4 inch display, transmissive, Normally Black
2.2 240(RGB) x 320 dots Matrix
2.3 Narrow-contact ledge technique.
2.4 262K: Red-6bit, Green-6bit, Blue-6bit (18-bit interface)
(3) Direct data display with display RAM
(4) Interface: MPU and RGB Interface. (Select by H/W Jumper).
Default: 80-16BIT Type II

	JP3(IM3)		**JP2(IM2)**		**JP1(IM1)**		**JP0(IM0)**		**Remark**
Interface mode	**1-2(H)**	**2-3(L)**	**1-2(H)**	**2-3(L)**	**1-2(H)**	**2-3(L)**	**1-2(H)**	**2-3(L)**	
80-8bit Parallel I/F	NC	0R	NC	0R	NC	0R	NC	0R	DB[7:0]
	0		0		0		0		
80-16bit Parallel I/F	NC	0R	NC	0R	NC	0R	0R	NC	DB[15:0]
	0		0		0		1		
80-9bit Parallel I/F	NC	0R	NC	0R	0R	NC	NC	0R	DB[8:0]
	0		0		1		0		
80-18bit Parallel I/F	NC	0R	NC	0R	0R	NC	0R	NC	DB[17:0]
	0		0		1		1		
3-line 9bit serial I/F 2 data lane serial I/F	NC	0R	0R	NC	NC	0R	0R	NC	SDA: in/out, WRX: in
	0		1		0		1		
4-line 8bit serial I/F	NC	0R	0R	NC	0R	NC	NC	0R	SDA: in/out
	0		1		1		0		
80-16bit Parallel I/F II	**0R**	**NC**	**NC**	**0R**	**NC**	**0R**	**NC**	**0R**	**DB[17:10],DB[8:1] Default**
	1		0		0		0		
80-8bit Parallel I/F II	0R	NC	NC	0R	NC	0R	0R	NC	DB[17:10]
	1		**0**		**0**		**1**		
80-18bit Parallel I/F II	0R	NC	NC	0R	0R	NC	NC	0R	DB[17:0]
	1		0		1		0		
80-9bit Parallel I/F II	0R	NC	NC	0R	0R	NC	0R	NC	DB[17:9]
	1		0		1		1		
3-line 9bit serial I/F II	0R	NC	0R	NC	NC	0R	0R	NC	SDA: in/ SDO: out
	1		1		0		1		
4-line 8bit serial I/F II	0R	NC	0R	NC	0R	NC	NC	0R	SDA: in/ SDO: out
	1		1		1		0		

2. Electrical specifications

2-1 Electrical characteristics of LCM

Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
IC power voltage(Power)	V_{DD}	Ta=25 °C	2.4	2.75	3.3	V
IC power voltage(Logic)	V_{DDI}	Ta=25 °C	1.65	1.8	3.3	V
High-level input voltage	V_{IH}	Ta=25 °C	$0.7V_{DDI}$		V_{DDI}	V
Low-level input voltage	V_{IL}	Ta=25 °C	GND		$0.3V_{DDI}$	V
Consumption current of VDD	I_{DD}	VDD=3.3V	-	8	15	mA

2-2 LED back light specification

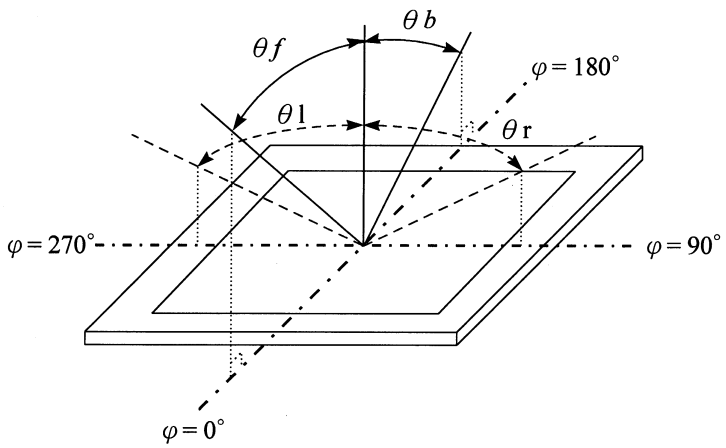
Item	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Forward voltage	V_f	I_f=T.B.D mA	-	T.B.D	-	V
Forward current	I_f	Ta=25 °C	-	T.B.D	-	mA
Luminous color	White					
LED connection	T.B.D					
LED life time	40Khrs (Estimated data, Ta=25℃)					

3. Optical Characteristics

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Viewing Angle	Front	θ_f	CR≧10	--	80	--	deg.	(1)(2)(3)
	Back	θ_b		--	80	--		
	Left	θ_l		--	80	--		
	Right	θ_r		--	80	--		
Contrast Ratio		CR	Θ=Φ=0°	640	800	--	--	(1)(3)
Response Time		T_r	Θ=Φ=0°	--	16	21	ms	(1)(4)
		T_f		--	19	24	ms	(1)(4)
Color chromaticity	White	Wx		0.24	0.29	0.34	--	(1)
		Wy		0.29	0.34	0.39		
	Red	Rx		0.55	0.60	0.65		
		Ry		0.28	0.33	0.38		
	Green	Gx		0.30	0.35	0.40		
		Gy		0.53	0.58	0.63		
	Blue	Bx		0.06	0.11	0.16		
		By		0.03	0.08	0.13		
Luminance		L	Θ=Φ=0°	250	320	--	cd/m^2	(1)(5)
Luminance Uniformity		ΔL	Θ=Φ=0°	--	70	--	%	(1)(5)(6)

Note 1: Ta=25°C. To be measured on the center area of panel after 10 minutes operation.

Note 2: Definition of Viewing Angle



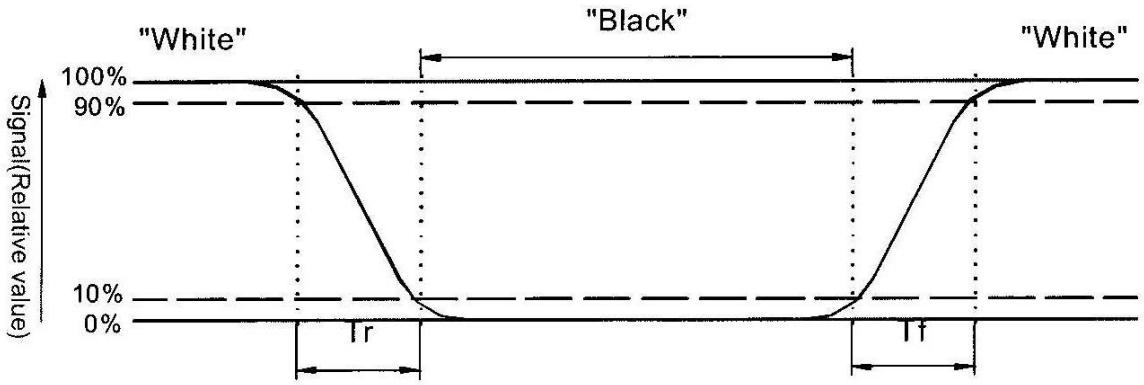
Note 3: Definition of contrast ratio:

Contrast ratio is calculated with the following formula.

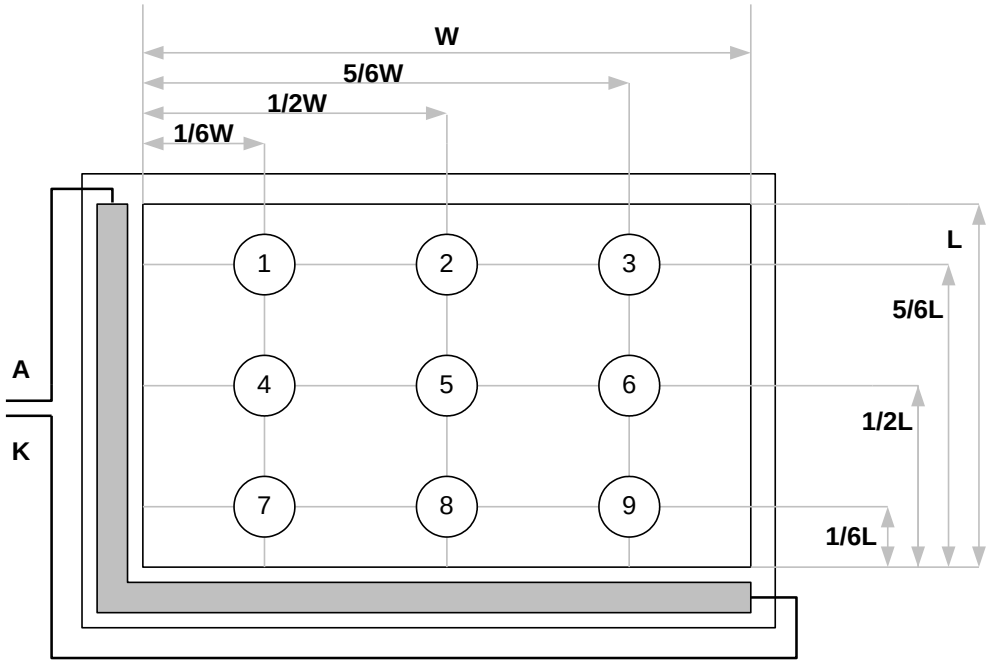
$$\text{Contrast ratio(CR)} = \frac{\text{Photo detector output when LCD is at ”White” state}}{\text{Photo detector Output when LCD is at “Black” state}}$$

Note 4: Definition of response time:

The output signals of photo detector are measured when the input signals are changed from “black“ to “white”(falling time) and from ”white” to “black” (rising time) respectively. The response time is defined as the time interval between the 10% and 90% of amplitudes. Refer to figure as below.



Note 5 : Luminance is measured at point 5 of the display.



Note 6 : Definition of Luminance Uniformity

ΔL = [L(min.) of 9 points / L(max.) of 9 points] X 100%

4. Interface Specifications

Pin No.	Terminal	Functions
1	ENABLE	A data ENABLE signal in RGB I/F mode.
2	DOTCLK	Dot clock signal in RGB I/F mode.
3	HSYNC	Frame synchronizing signal in RGB I/F mode.
4	VSYNC	Frame synchronizing signal in RGB I/F mode.
5	/CS	**- Connect to IC ST7789V CSX** - Chip selection pin Low enable. High disable.
6	WR/SCL	**- Connect to IC ST7789V DCX** - Display data/command selection pin in parallel interface. - This pin is used to be serial interface clock. DCX='1': display data or parameter. DCX='0': command data. - If not used, please fix this pin at VDD or GND.
7	SDI	**- Connect to IC ST7789V SDA** - IM3: High, SPI interface input pin. - IM3: LOW, SPI interface input/output pin. - **The data is latched on the rising edge of the SCL signal.** - If not used, please fix this pin at VDD or GND.
8	RS	**- Connect to IC ST7789V WRX** - Write enable in MCU parallel interface. - Display data/command selection pin in 4-line serial interface. - Second Data lane in 2 data lane serial interface. - If not used, please fix this pin at VDD or GND.
9	NC	NC
10	/RD	**- Connect to IC ST7789V RDX** - Read enable in 8080 MCU parallel interface. - If not used, please fix this pin at VCC or GND.
11	/RESET	Reset pin. Setting either pin low initializes the LSI. Must be reset the chop after power being supplied.
12	PD0	
13	PD1	
14	PD2	
15	PD3	
16	PD4	
17	PD5	
18	PD6	
19	PD7	
20	PD8	
21	PD9	
22	PD10	
23	PD11	
24	PD12	
25	PD13	
26	PD14	
27	PD15	
28	PD16	
29	PD17	

IM3	IM2	IM1	IM0	MPU Interface Mode	Data pin
0	0	0	0	80-8bit parallel I/F	DB[7:0]
0	0	0	1	80-16bit parallel I/F	DB[15:0]
0	0	1	0	80-9bit parallel I/F	DB[8:0]
0	0	1	1	80-18bit parallel I/F	DB[17:0],
0	1	0	1	3-line 9bit serial I/F	SDA: in/out
0	1	1	0	4-line 8bit serial I/F	SDA: in/out
1	0	0	0	80-16bit parallel I/F Ⅱ	DB[17:10], DB[8:1]
1	0	0	1	80-8bit parallel I/F Ⅱ	DB[17:10]
1	0	1	0	80-18bit parallel I/F Ⅱ	DB[17:0],
1	0	1	1	80-9bit parallel I/F Ⅱ	DB[17:9]
1	1	0	1	3-line 9bit serial I/F Ⅱ	SDA:in/ SDO: out
1	1	1	0	4-line 8bit serial I/F Ⅱ	SDA:in/ SDO: out

30	VDD	Power supply for the internal logic circuit. (VDD=2.4~3.3V)
31	VCI	Power supply for interface I/O. (VDDI=1.65~3.3V)
32	VCI	
33	NC	NC
34	NC	
35	NC	
36	NC	
37	NC	
38	NC	
39	NC	
40	GND	GND-terminal
41	NC	NC
42	NC	
43	NC	
44	NC	
45	GND	GND-terminal
46	GND	GND-terminal
47	NC	NC
48	NC	
49	NC	
50	GND	GND-terminal
51	GND	

5. Function Description

5.1 8080-II Series MCU Parallel Interface

The MCU uses one of following interface: 11-lines with 8-data parallel interface, 12-lines with 9-data parallel interface, 19-lines with 16-data parallel interface, or 21-lines with 18-data parallel interface. The chip-select CSX(active low) enables and disables the parallel interface. RESX (active low) is an external reset signal. The R/WX is the Read/Write flag and D[17:0] is parallel data bus.

The LCD driver reads the data at the rising edge of WRX signal. The D/CX is the data/command flag. When D/CX='1', D[17:0] bits is either display data or command parameter. When D/C='0', D[17:0] bits is command.

The 8080-Ⅱ series bi-directional interface can be used for communication between the micro controller and LCD driver. Interface bus width can be selected with IM3, IM2, IM1 and IM0.The interface functions of 8080-Ⅱ series parallel interface are given in Table 12 The function of 8080-Ⅱ series parallel interface.

IM3	IM2	IM1	IM0	Interface	D/CX	RDX	WRX	Function
1	0	0	0	16-bit Parallel	0	1	↑	Write 8-bit command (D[8:1])
					1	1	↑	Write 16-bit display data or 8-bit parameter (D[17:10], D[8:1])
					1	↑	1	Read 16-bit Display data (D[17:10], D[8:1])
					1	↑	1	Read 8-bit parameter or status (D[8:1])
1	0	0	1	8-bit Parallel	0	1	↑	Write 8-bit command (D[17:10])
					1	1	↑	Write 8-bit display data or 8-bit parameter (D[17:10])
					1	↑	1	Read 8-bit Display data (D[17:10])
					1	↑	1	Read 8-bit parameter or status (D[17:10])
1	0	1	0	18-bit Parallel	0	1	↑	Write 8-bit command (D[8:1])
					1	1	↑	Write 18-bit display data or 8-bit parameter (D[17:0], D[8:1])
					1	↑	1	Read 18-bit Display data (D[17:0])
					1	↑	1	Read 8-bit parameter or status (D[8:1])
1	0	1	1	9-bit Parallel	0	1	↑	Write 8-bit command (D[17:10])
					1	1	↑	Write 9-bit display data or 8-bit parameter (D[17:9])
					1	↑	1	Read 9-bit Display data (D[17:9])
					1	↑	1	Read 8-bit parameter or status (D[17:10])

Table 12 The function of 8080-II series parallel interface

5.1.1 Write cycle sequence

The write cycle means that the host writes information (command / data) to the display via the interface. Each write cycle (WRX high-low-high sequence) consists of 3 control signals (DCX, RDX, WRX) and data signals (DB[17:0]). DCX bit is a control signal, which tells if the data is a command or a data. The data signals are the command if the control signal is low (='0') and vice versa it is data (='1').

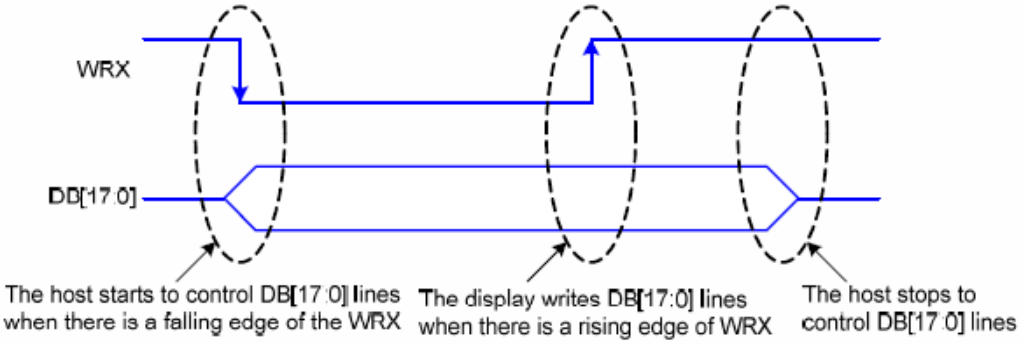


Figure 8 8080-Series WRX Protocol

Note: WRX is an unsynchronized signal (It can be stopped).

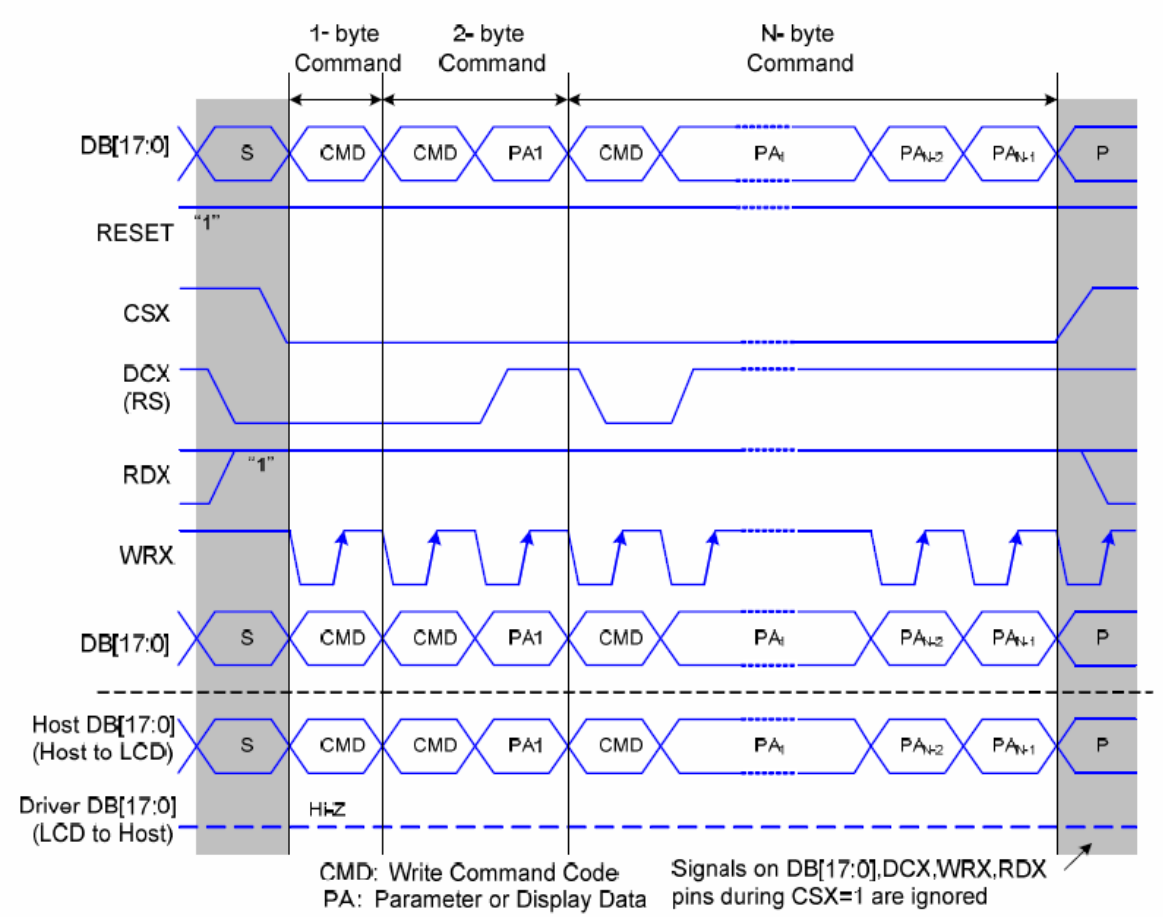


Figure 9 8080-Series Parallel Bus Protocol, Write to Register or Display RAM

5.1.2 Read cycle sequence

The read cycle (RDX high-low-high sequence) means that the host reads information from LCD driver via interface. The driver sends data (D[17:0]) to the host when there is a falling edge of RDX and the host reads data when there is a rising edge of RDX.

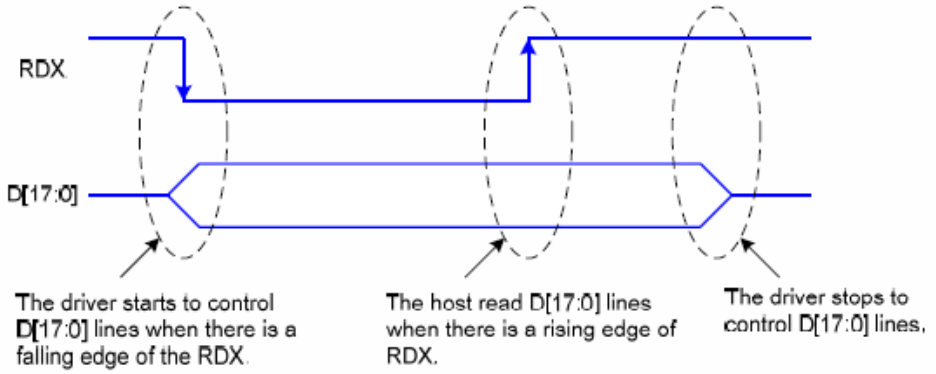


Figure 10 8080-series RDX protocol

Note: RDX is an unsynchronized signal (It can be stopped).

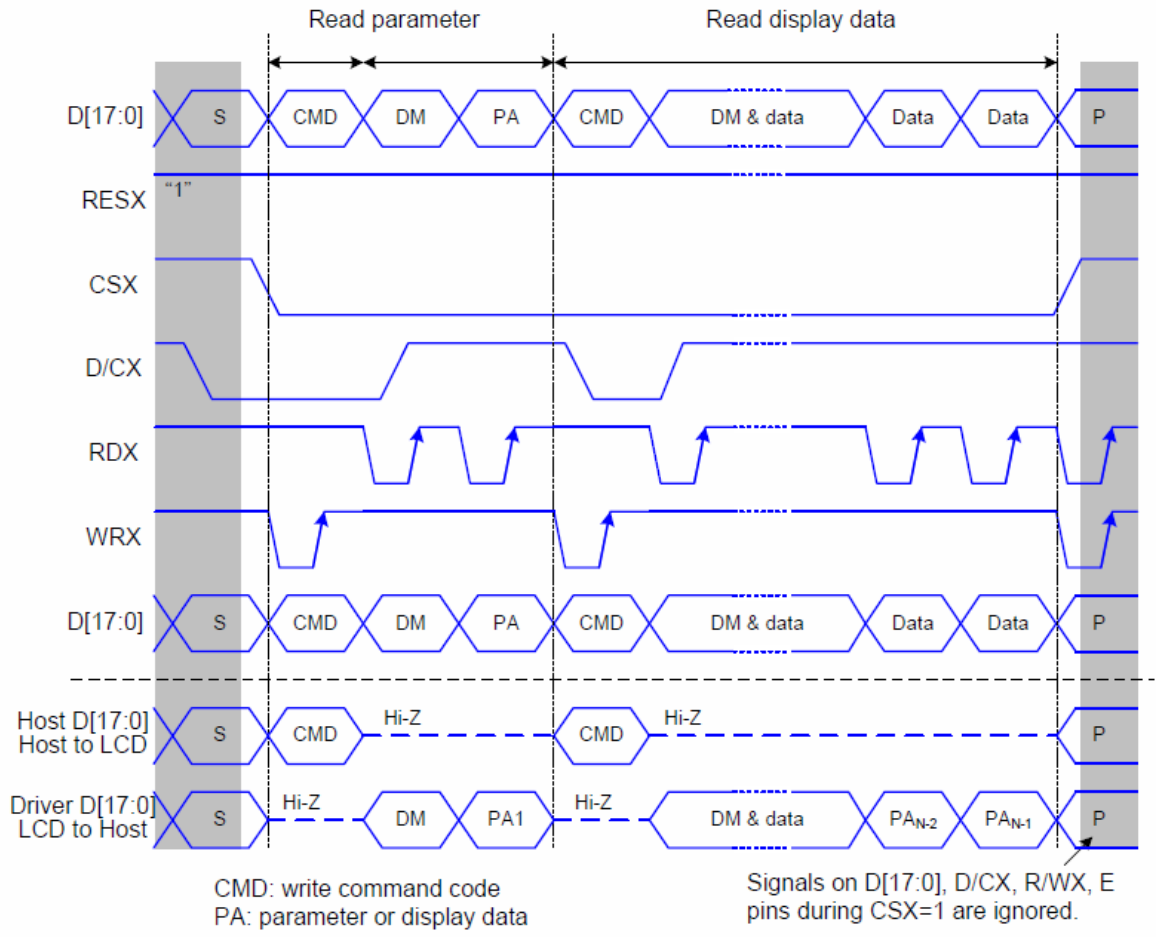


Figure 11 8080-series parallel bus protocol, read data from register or display RAM

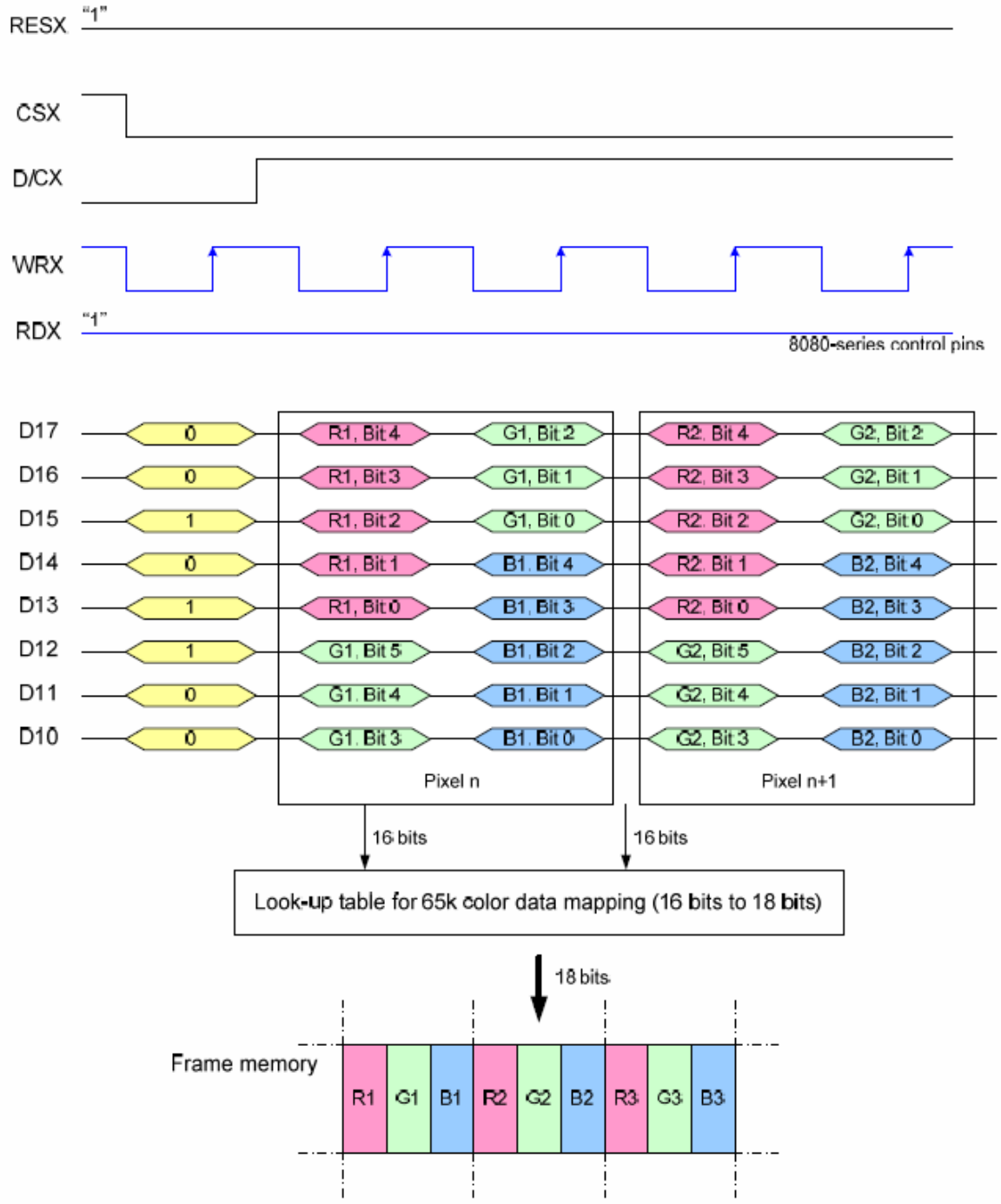
6. Data Color Coding

6.1 8080-II Series 8-bit Parallel Interface

The 8080-Ⅱ series 8-bit parallel interface of ST7789V2 can be used by setting IM[3:0]="1001b". Different display data formats are available for three Colors depth supported by listed below.

- 65k colors, RGB 5,6,5-bit input.
- 262k colors, RGB 6,6,6-bit input.

6.2 8-bit data bus for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors, 3Ah="05h"

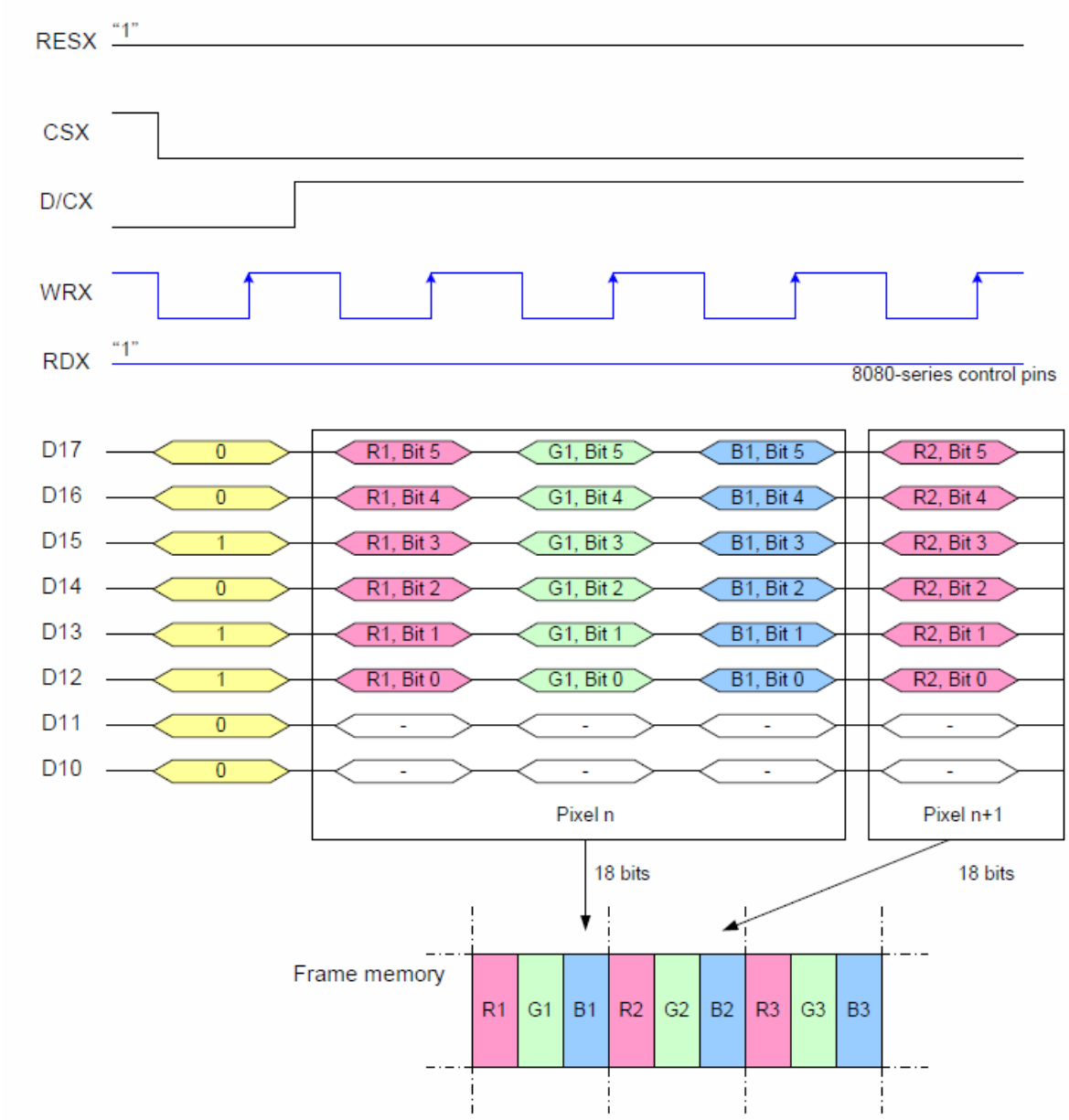


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Green, and MSB=Bit 4, LSB=Bit 0 for Red and Blue data.

Note 2: 2-times transfer transmit 1 pixel data with the 16-bit color depth information.

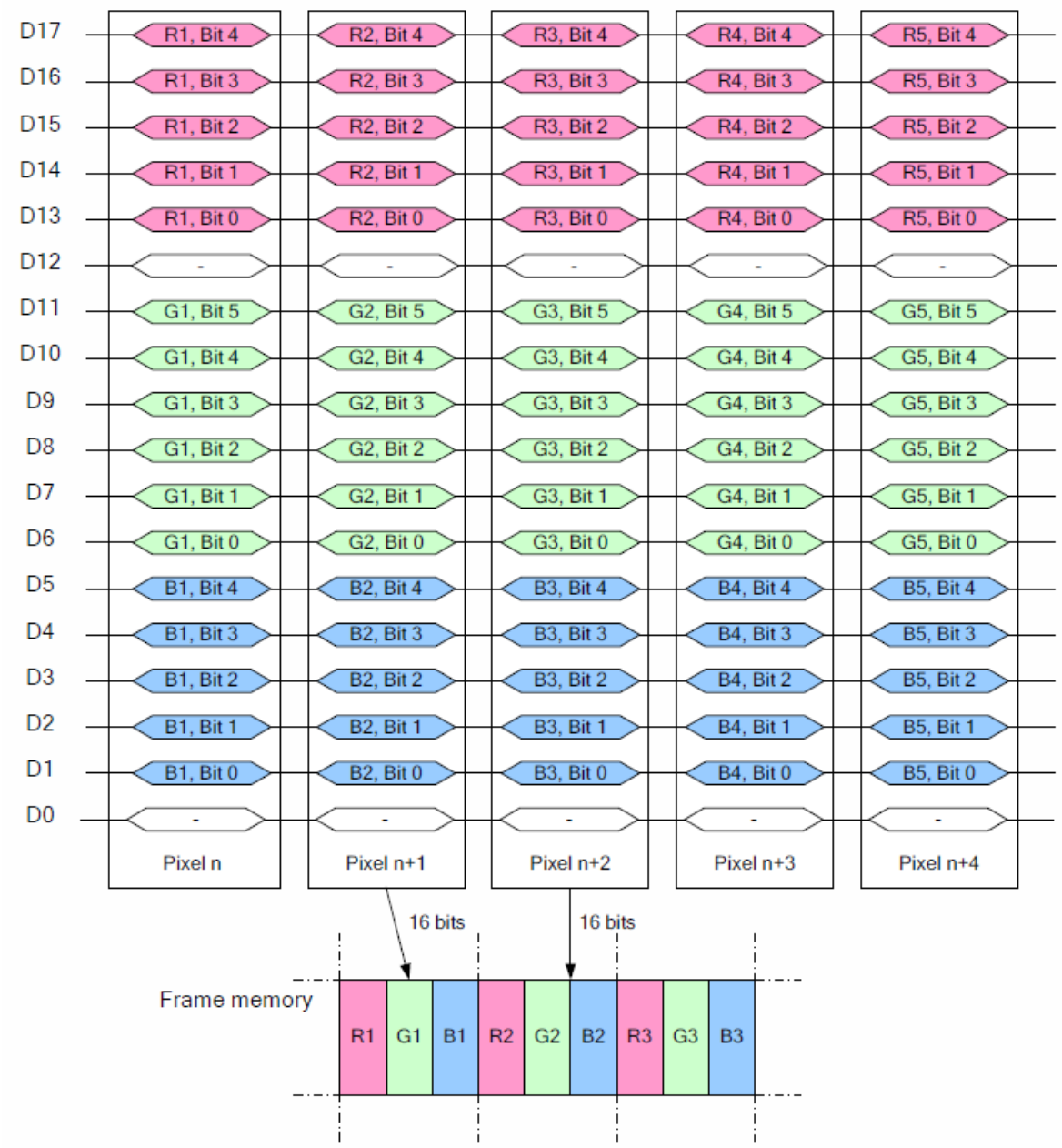
Note 3: '-' = Don't care – Can be set to '0' or '1'

6.3 8-bit data bus for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors, 3Ah=”06h”

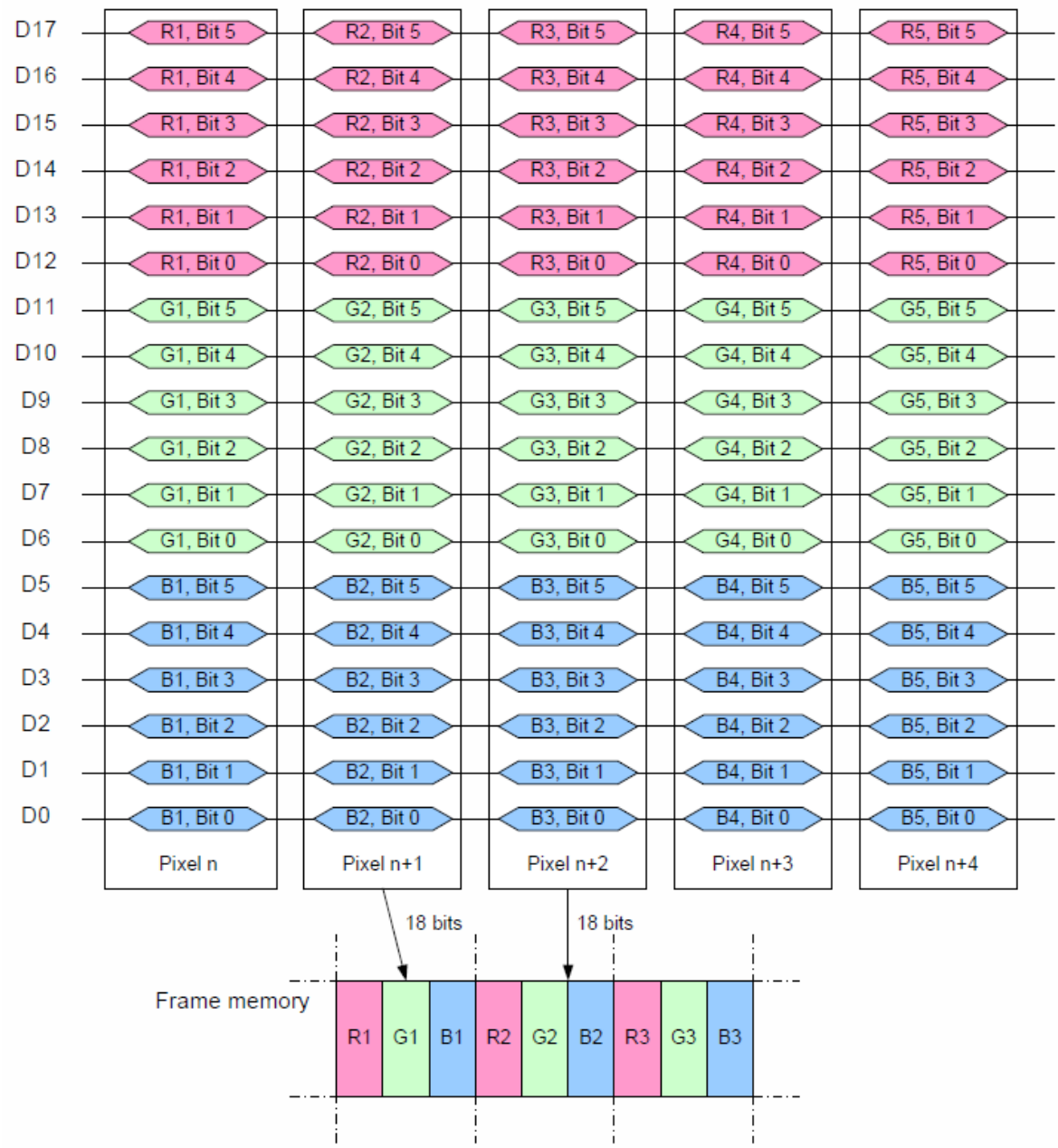


Note 1: The data order is as follows, MSB=D17, LSB=D10 and picture data is MSB=Bit 5, LSB=Bit 0 for Red, Green and Blue data.
Note 2: 3-times transfer is used to transmit 1 pixel data with the 18-bit color depth information.
Note 3: '-' = Don't care – Can be set to '0' or '1'

6.4 Write data for 16-bit/pixel (RGB 5-6-5-bit input), 65K-Colors



6.5 Write data for 18-bit/pixel (RGB 6-6-6-bit input), 262K-Colors



7. AC Characteristics

7.1 8080 Series MCU Parallel Interface Characteristics: 18/16/9/8-bit Bus

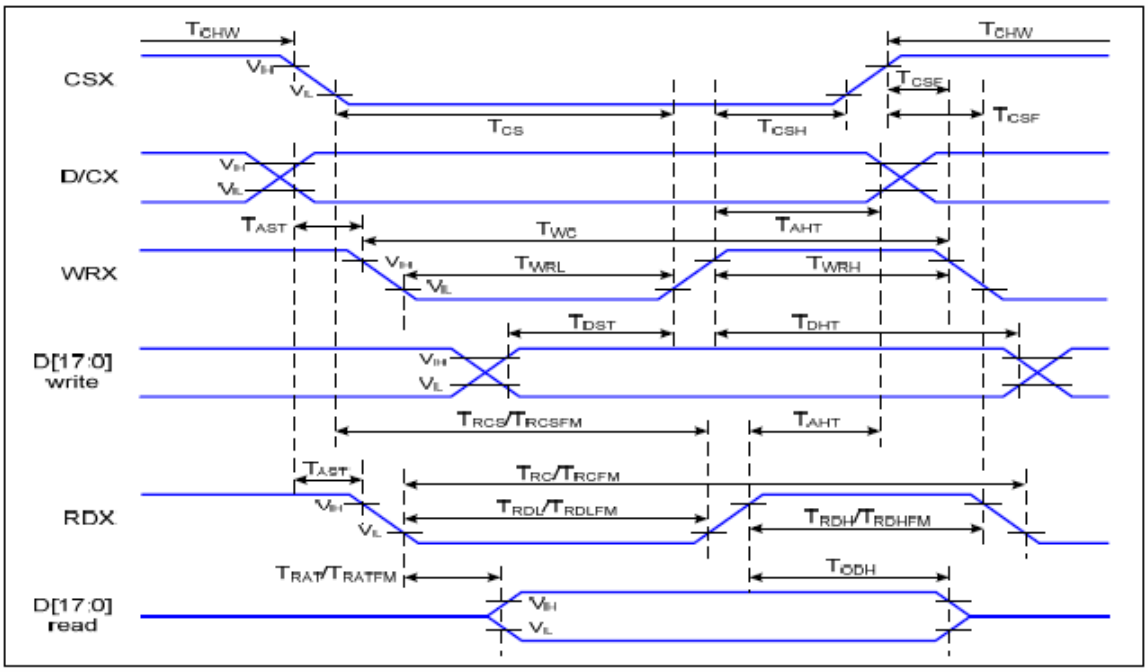


Figure 1 Parallel Interface Timing Characteristics (8080-Series MCU Interface)

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Signal	Symbol	Parameter	Min	Max	Unit	Description
D/CX	T_{AST}	Address setup time	0		ns	-
	T_{AHT}	Address hold time (Write/Read)	10		ns	
CSX	T_{CHW}	Chip select "H" pulse width	0		ns	-
	T_{CS}	Chip select setup time (Write)	15		ns	
	T_{RCS}	Chip select setup time (Read ID)	45		ns	
	T_{RCSFM}	Chip select setup time (Read FM)	355		ns	
	T_{CSF}	Chip select wait time (Write/Read)	10		ns	
	T_{CSH}	Chip select hold time	10		ns	
WRX	T_{WC}	Write cycle	66		ns	
	T_{WRH}	Control pulse "H" duration	15		ns	
	T_{WRL}	Control pulse "L" duration	15		ns	
RDX (ID)	T_{RC}	Read cycle (ID)	160		ns	When read ID data
	T_{RDH}	Control pulse "H" duration (ID)	90		ns	
	T_{RDL}	Control pulse "L" duration (ID)	45		ns	
RDX (FM)	T_{RCFM}	Read cycle (FM)	450		ns	When read from frame memory
	T_{RDHFM}	Control pulse "H" duration (FM)	90		ns	
	T_{RDLFM}	Control pulse "L" duration (FM)	355		ns	
D[17:0]	T_{DST}	Data setup time	10		ns	For CL=30pF

	T_{DHT}	Data hold time	10		ns	
	T_{RAT}	Read access time (ID)		40	ns	
	T_{RATFM}	Read access time (FM)		340	ns	
	T_{ODH}	Output disable time	20	80	ns	

Table 4 8080 Parallel Interface Characteristics

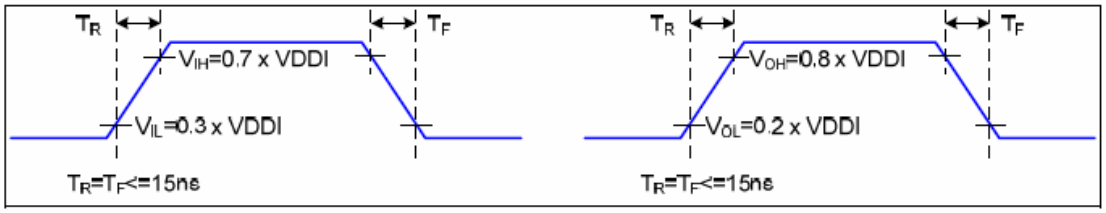


Figure 2 Rising and Falling Timing for I/O Signal

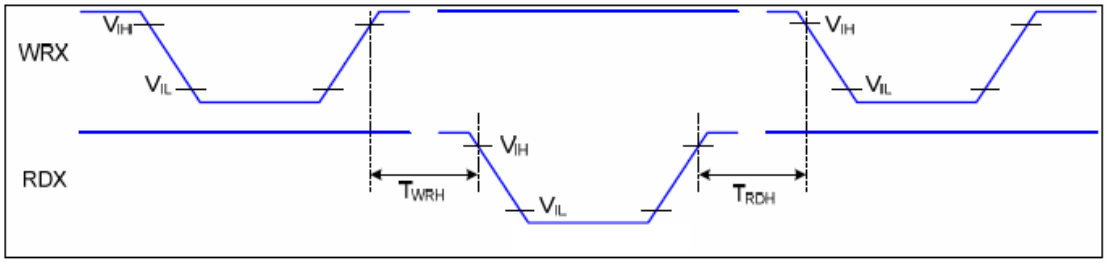


Figure 3 Write-to-Read and Read-to-Write Timing

Note: The rising time and falling time (Tr, Tf) of input signal and fall time are specified at 15 ns or less. Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.

7.2 Reset Timing

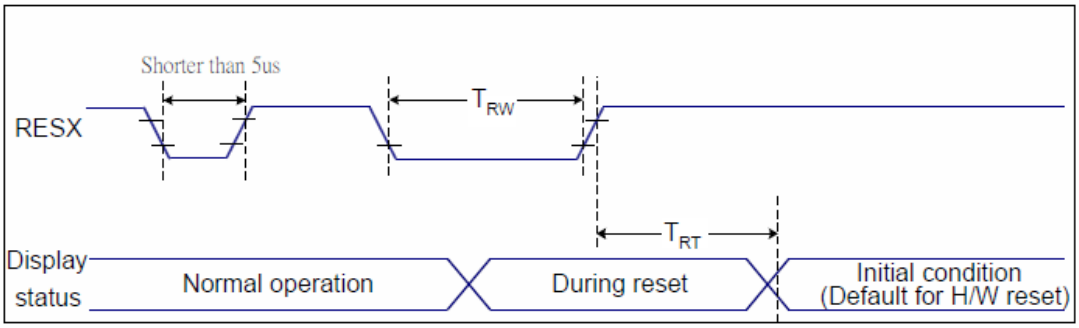


Figure 7 Reset Timing

VDDI=1.65 to 3.3V, VDD=2.4 to 3.3V, AGND=DGND=0V, Ta=25℃

Related Pins	Symbol	Parameter	MIN	MAX	Unit
RESX	TRW	Reset pulse duration	10	-	us
	TRT	Reset cancel	-	5 (Note 1, 5)	ms
				120 (Note 1, 6, 7)	ms

Table 9 Reset Timing

Notes:

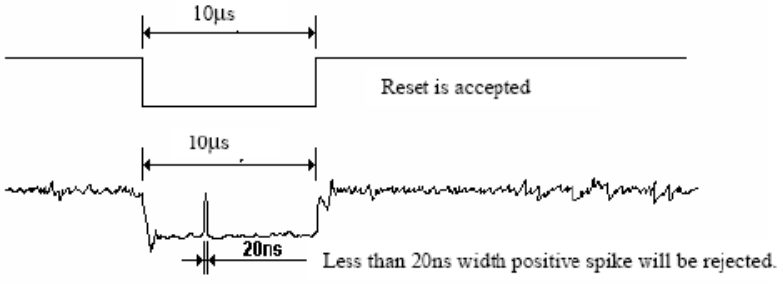
1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from NVM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below:

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In –mode.) and then return to Default condition for Hardware Reset.

4. Spike Rejection also applies during a valid reset pulse as shown below:



5. When Reset applied during Sleep In Mode.

6. When Reset applied during Sleep Out Mode.

7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

8. Power Level Definition

8.1 Power Level

6 level modes are defined they are in order of Maximum Power consumption to Minimum Power Consumption

1. Normal Mode On (full display), Idle Mode Off, Sleep Out.
   In this mode, the display is able to show maximum 262,144 colors.

2. Partial Mode On, Idle Mode Off, Sleep Out.
   In this mode part of the display is used with maximum 262,144 colors.

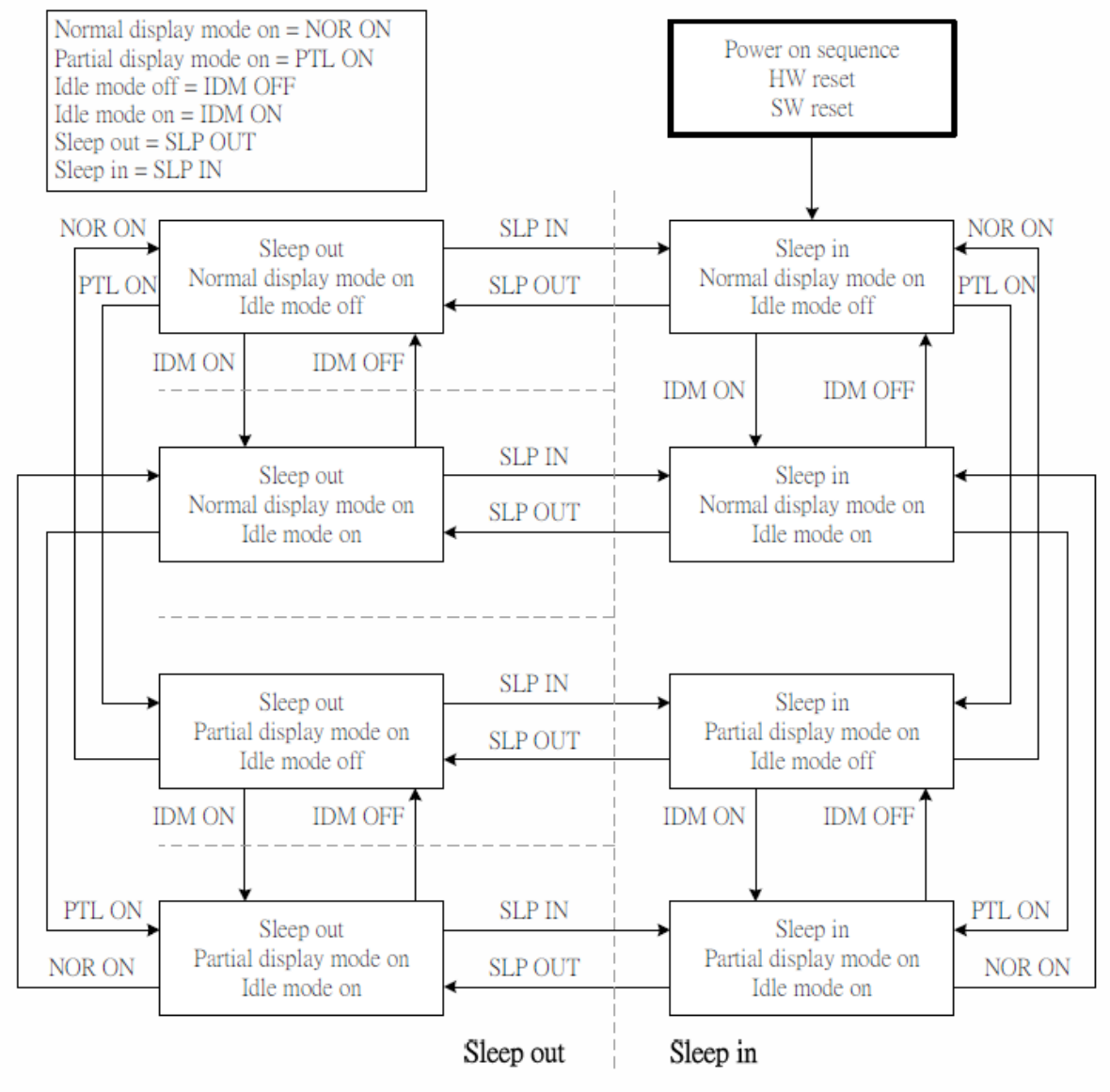
3. Normal Mode On (full display), Idle Mode On, Sleep Out.
   In this mode, the full display area is used but with 8 colors.

4. Partial Mode On, Idle Mode On, Sleep Out.
   In this mode, part of the display is used but with 8 colors.

5. Sleep In Mode
   In this mode, the DC: DC converter, internal oscillator and panel driver circuit are stopped. Only the MCU interface and memory works with VDDI power supply. Contents of the memory are safe.

Note: Transition between modes 1-5 is controllable by MCU commands. Mode 6 is entered only when both Power supplies are removed.

8.2 Power Flow Chart



9. Command Table

9.1 System Function Command Table 1

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
NOP	0	↑	1	-	0	0	0	0	0	0	0	0	(00h)	No operation
SWRESET	0	↑	1	-	0	0	0	0	0	0	0	1	(01h)	Software reset
RDDID	0	↑	1	-	0	0	0	0	0	1	0	0	(04h)	Read display ID
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		ID1 read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		ID2 read
	1	1	↑	-	ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		ID3 read
RDDST	0	↑	1	-	0	0	0	0	1	0	0	1	(09h)	Read display status
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	MY	MX	MV	ML	RGB	MH	ST24		-
	1	1	↑	-	ST23	IFPF2	IFPF1	IFPF0	IDMON	PTLON	SLOUT	NORON		-
	1	1	↑	-	ST15	ST14	INVON	ST12	ST11	DISON	TEON	GCS2		-
	1	1	↑	-	GCS1	GCS0	TEM	ST4	ST3	ST2	ST1	ST0		-
RDDPM	0	↑	1	-	0	0	0	0	1	0	1	0	(0Ah)	Read display power
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	BSTON	IDMON	PTLON	SLPOUT	NORON	DISON	0	0		
RDD MADCTL	0	↑	1	-	0	0	0	0	1	0	1	1	(0Bh)	Read display
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	MY	MX	MV	ML	RGB	MH	0	0		-
RDD COLMOD	0	↑	1	-	0	0	0	0	1	1	0	0	(0Ch)	Read display pixel
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	D6	D5	D4	0	D2	D1	D0		-
RDDIM	0	↑	1	-	0	0	0	0	1	1	0	1	(0Dh)	Read display image
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	VSSON	0	INVON	0	0	GC2	GC1	GC0		-
RDDSM	0	↑	1	-	0	0	0	0	1	1	1	0	(0Eh)	Read display signal
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	TEON	TEM	0	0	0	0	0	0		-
RDDSDR	0	↑	1	-	0	0	0	0	1	1	1	1	(0Fh)	Read display self-diagnostic result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
SLPIN	0	↑	1	-	0	0	0	1	0	0	0	0	(10h)	Sleep in
SLPOUT	0	↑	1	-	0	0	0	1	0	0	0	1	(11h)	Sleep out
PTLON	0	↑	1	-	0	0	0	1	0	0	1	0	(12h)	Partial mode on
NORON	0	↑	1	-	0	0	0	1	0	0	1	1	(13h)	Partial off (Normal)
INVOFF	0	↑	1	-	0	0	1	0	0	0	0	0	(20h)	Display inversion off
INVON	0	↑	1	-	0	0	1	0	0	0	0	1	(21h)	Display inversion on
GAMSET	0	↑	1	-	0	0	1	0	0	0	0	1	(26h)	Display inversion on
	1	↑	1	-	0	0	0	0	GC3	GC2	GC1	GC0		
DISPOFF	0	↑	1	-	0	0	1	0	1	0	0	0	(28h)	Display off
DISPON	0	↑	1	-	0	0	1	0	1	0	0	1	(29h)	Display on
CASET	0	↑	1	-	0	0	1	0	1	0	1	0	(2Ah)	Column address set
	1	↑	1	-	XS15	XS14	XS13	XS12	XS11	XS10	XS9	XS8		X address start:
	1	↑	1		XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0		0≤XS≤X
	1	↑	1		XE15	XE14	XE13	XE12	XE11	XE10	XE9	XE8		X address start:
	1	↑	1		XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0		S≤XE≤X
RASET	0	↑	1	-	0	0	1	0	1	0	1	1	(2Bh)	Row address set
	1	↑	1	-	YS15	YS14	YS13	YS12	YS11	YS10	YS9	YS8		Y address start:
	1	↑	1		YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0		0≤YS≤Y
	1	↑	1		YE15	YE14	YE13	YE12	YE11	YE10	YE9	YE8		Y address start:
	1	↑	1		YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0		S≤YE≤Y
RAMWR	0	↑	1	-	0	0	1	0	1	1	0	0	(2Ch)	Memory write
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRD	0	↑	1	-	0	0	1	0	1	1	1	0	(2Eh)	Memory read

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Read data
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
PTLAR	0	↑	1	-	0	0	1	1	0	0	0	0	(30h)	Partial sart/end address set
	1	↑	1	-	PSL15	PSL14	PSL13	PSL12	PSL11	PSL10	PSL9	PSL8		Partial start address: (0, 1,2, ..P)
	1	↑	1	-	PSL7	PSL6	PSL5	PSL4	PSL3	PSL2	PSL1	PSL0		
	1	↑	1	-	PEL15	PEL14	PEL13	PEL12	PEL11	PEL10	PEL9	PEL8		Partial end address (0, 1,2, 3, , P)
	1	↑	1	-	PEL7	PEL6	PEL5	PEL4	PEL3	PEL2	PEL1	PEL0		
VSCRDEF	0	↑	1	-	0	0	1	1	0	0	1	1	(33h)	Vertical scrolling definition
	1	↑	1	-	TFA15	TFA14	TFA13	TFA12	TFA11	TFA10	TFA9	TFA8		
	1	↑	1	-	TFA7	TFA6	TFA5	TFA4	TFA3	TFA2	TFA1	TFA0		
	1	↑	1	-	VSA15	VSA14	VSA13	VSA12	VSA11	VSA10	VSA9	VSA8		
	1	↑	1	-	VSA7	VSA6	VSA5	VSA4	VSA3	VSA2	VSA1	VSA0		
	1	↑	1	-	BFA15	BFA14	BFA13	BFA12	BFA11	BFA10	BFA9	BFA8		
	1	↑	1	-	BFA7	BFA6	BFA5	BFA4	BFA3	BFA2	BFA1	BFA0		
TEOFF	0	↑	1	-	0	0	1	1	0	1	0	0	(34h)	Tearing effect line off
TEON	0	↑	1	-	0	0	1	1	0	1	0	1	(35h)	Tearing effect line on
	1	↑	1	-	-	-	-	-	-	-	-	TEM		
MADCTL	0	↑	1	-	0	0	1	1	0	1	1	0	(36h)	Memory data access control
	1	↑	1	-	MY	MX	MV	ML	RGB	0	0	0		-
VSCRSADD	0	↑	1	-	0	0	1	1	0	1	1	1	(37h)	Vertical scrolling start address
	1	↑	1	-	VSP15	VSP14	VSP13	VSP12	VSP11	VSP10	VSP9	VSP8		
	1	↑	1	-	VSP7	VSP6	VSP5	VSP4	VSP3	VSP2	VSP1	VSP0		
IDMOFF	0	↑	1	-	0	0	1	1	1	0	0	0	(38h)	Idle mode off
IDMON	0	↑	1	-	0	0	1	1	1	0	0	1	(39h)	Idle mode on

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
COLMOD	0	↑	1	-	0	0	1	1	1	0	1	0	(3Ah)	Interface pixel format
	1	↑	1	-	0	D6	D5	D4	0	D2	D1	D0		Interface format
RAMWRC	0	↑	1	-	0	0	1	1	1	1	0	0	(3Ch)	Memory write continue
	1	↑	1	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		Write data
	1	↑	1	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	↑	1	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
RAMRDC	0	↑	1	-	0	0	1	1	1	1	1	0	(3Eh)	Memory read continue
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	D1[17:8]	D1[7]	D1[6]	D1[5]	D1[4]	D1[3]	D1[2]	D1[1]	D1[0]		
	1	1	↑	Dx[17:8]	Dx[7]	Dx[6]	Dx[5]	Dx[4]	Dx[3]	Dx[2]	Dx[1]	Dx[0]		
	1	1	↑	Dn[17:8]	Dn[7]	Dn[6]	Dn[5]	Dn[4]	Dn[3]	Dn[2]	Dn[1]	Dn[0]		
TESCAN	0	↑	1	-	0	1	0	0	0	1	0	0	(44h)	Set tear scanline
	1	↑	1	-	N15	N14	N13	N12	N11	N10	N9	N8		
	1	↑	1	-	N7	N6	N5	N4	N3	N2	N1	N0		
RDTESCAN	0	↑	1	-	0	1	0	0	0	1	0	1	(45h)	Get scanline
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy Read
	1	1	↑	-	-	-	-	-	-	-	N9	N8		
	1	1	↑	-	N7	N6	N5	N4	N3	N2	N1	N0		
WRDISBV	0	↑	1	-	0	1	0	1	0	0	0	1	(51h)	Write display brightness
	1	↑	1	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
RDDISBV	0	↑	1	-	0	1	0	1	0	0	1	0	(52h)	Read display brightness value
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	DBV7	DBV6	DBV5	DBV4	DBV3	DBV2	DBV1	DBV0		
WRCTRLD	0	↑	1	-	0	1	0	1	0	0	1	1	(53h)	Write CTRL display
	1	↑	1	-	0	0	BCTRL	0	DD	BL	0	0		
RDCTRLD	0	↑	1	-	0	1	0	1	0	1	0	0	(54h)	Read CTRL value dsiplay
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	0	BCTRL	0	DD	BL	0	0		

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
WRCACE	0	↑	1	-	0	1	0	1	0	1	0	1	(55h)	Write content adaptive brightness control and Color enhancemnet
	1	↑	1	-	CECTRL	0	CE1	CE0	0	0	C1	C0		
RDCABC	0	↑	1	-	0	1	0	1	0	1	1	0	(56h)	Read content adaptive brightness control
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	0	CECTRL	0	0	0	0	C1	C0		
WRCABCMB	0	↑	1	-	0	1	0	1	1	1	1	0	(5Eh)	Write CABC minimum brightness
	1	↑	1	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDCABCMB	0	↑	1	-	0	1	0	1	1	1	1	1	(5Fh)	Read CABC minimum brightness
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0		
RDABCSDR	0	↑	1	-	0	1	1	0	1	0	0	0	(68h)	Read Automatic Brightness Control Self-Diagnostic Result
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	D7	D6	0	0	0	0	0	0		-
RDID1	0	↑	1	-	1	1	0	1	1	0	1	0	(Dah)	Read ID1
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID17	ID16	ID15	ID14	ID13	ID12	ID11	ID10		Read parameter
RDID2	0	↑	1	-	1	1	0	1	1	0	1	1	(DBh)	Read ID2
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑	-	ID27	ID26	ID25	ID24	ID23	ID22	ID21	ID20		Read parameter
RDID3	0	↑	1	-	1	1	0	1	1	1	0	0	(DCh)	Read ID3

Instruction	D/CX	WRX	RDX	D17-8	D7	D6	D5	D4	D3	D2	D1	D0	Hex	Function
	1	1	↑	-	-	-	-	-	-	-	-	-		Dummy read
	1	1	↑		ID37	ID36	ID35	ID34	ID33	ID32	ID31	ID30		Read parameter

Table 19 System Function Command List

"-": Don't care

10. RELIABILITY

Test Item	Test Conditions	Note
High Temperature Operation	70±3°C , t=240 hrs	
Low Temperature Operation	-20±3°C , t=240 hrs	
High Temperature Storage	80±3°C , t=240 hrs	1,2
Low Temperature Storage	-30±3°C , t=240 hrs	1,2
Thermal Shock Test	-20°C ~ 25°C ~ 70°C 30 m in. 5 min. 30 min. (1 cycle) total 5 cycle	1,2
Storage Humidity Test	60 °C, Humidity 90%, 96 hrs	1,2
Vibration Test (Packing)	Sweep frequency : 10 ~ 55 ~ 10 Hz/1min Amplitude : 0.75mm Test direction : X.Y.Z/3 axis Duration : 30min/each axis	2

Note 1 : Condensation of water is not permitted on the module.

Note 2 : The module should be inspected after 1 hour storage in normal conditions (15-35°C , 45-65%RH).

Note 3 : The module shouldn't be tested more than one condition, and all the test conditions are independent.

Note 4 : All the reliability tests should be done without protective film on the module.

Definitions of life end point :

- Current drain should be smaller than the specific value.
- Function of the module should be maintained.
- Appearance and display quality should not have degraded noticeably.
- Contrast ratio should be greater than 50% of the initial value.

11. USE PRECAUTIONS

11-1 Handling precautions

1) The polarizing plate may break easily so be careful when handling it. Do not touch, press or rub it with a hard-material tool like tweezers.
2) Do not touch the polarizing plate surface with bare hands so as not to make it dirty. If the surface or other related part of the polarizing plate is dirty, soak a soft cotton cloth or chamois leather in benzine and wipe off with it. Do not use chemical liquids such as acetone, toluene and isopropyl alcohol. Failure to do so may bring chemical reaction phenomena and deteriorations.
3) Remove any spit or water immediately. If it is left for hours, the suffered part may deform or decolorize.
4) If the LCD element breaks and any LC stuff leaks, do not suck or lick it. Also if LC stuff is stuck on your skin or clothing, wash thoroughly with soap and water immediately.

11-2 Installing precautions

1) The PCB has many ICs that may be damaged easily by static electricity. To prevent breaking by static electricity from the human body and clothing, earth the human body properly using the high resistance and discharge static electricity during the operation. In this case, however, the resistance value should be approx. 1MΩ and the resistance should be placed near the human body rather than the ground surface. When the indoor space is dry, static electricity may occur easily so be careful. We recommend the indoor space should be kept with humidity of 60% or more. When a soldering iron or other similar tool is used for assembly, be sure to earth it.
2) When installing the module and ICs, do not bend or twist them. Failure to do so may crack LC element and cause circuit failure.
3) To protect LC element, especially polarizing plate, use a transparent protective plate (e.g., acrylic plate, glass etc) for the product case.
4) Do not use an adhesive like a both-side adhesive tape to make LCD surface (polarizing plate) and product case stick together. Failure to do so may cause the polarizing plate to peel off.

11-3 Storage precautions

1) Avoid a high temperature and humidity area. Keep the temperature between 0°C and 35°C and also the humidity under 60%.
2) Choose the dark spaces where the product is not exposed to direct sunlight or fluorescent light.
3) Store the products as they are put in the boxes provided from us or in the same conditions as we recommend.

11-4 Operating precautions

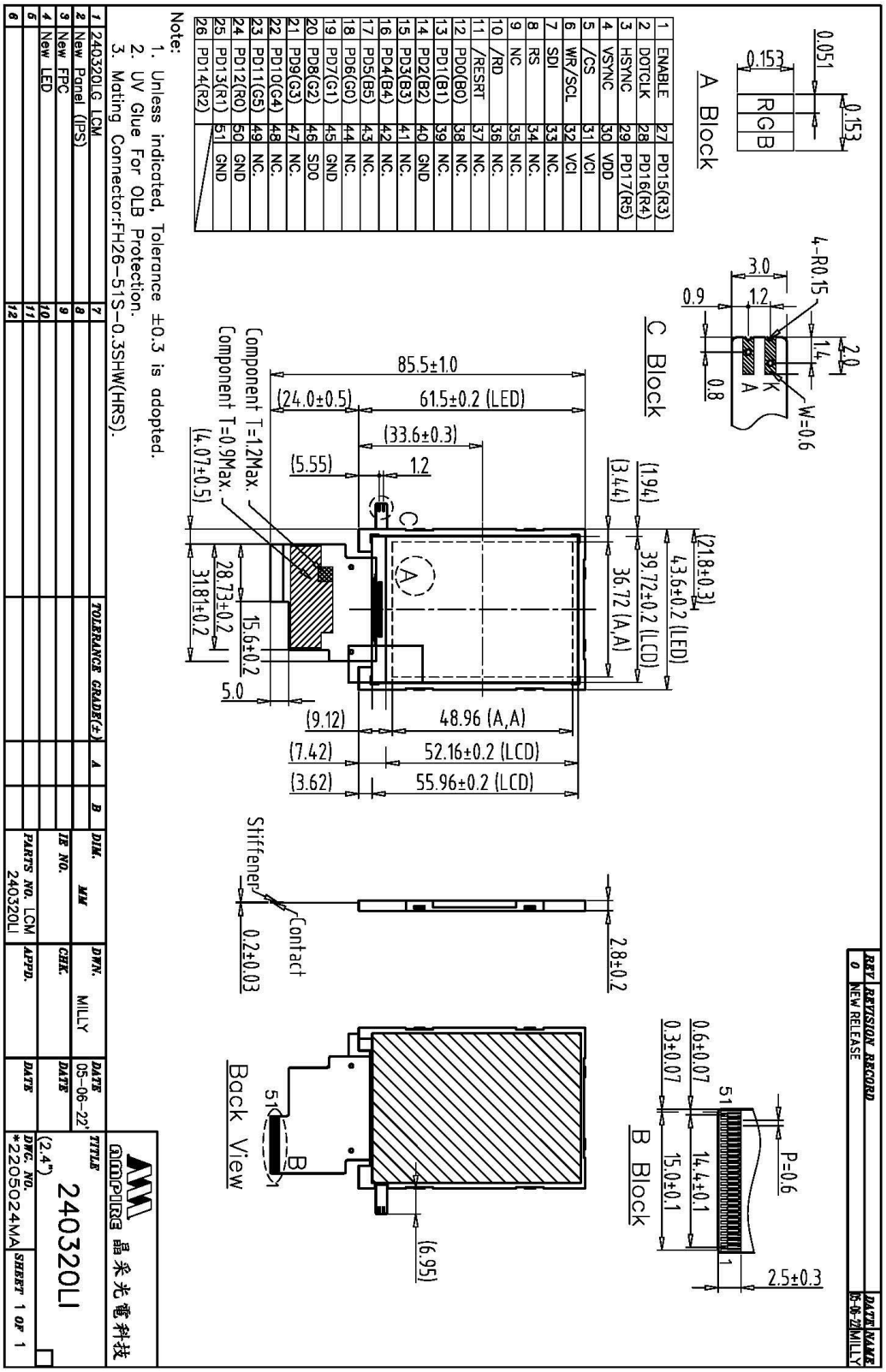
1) Do not boost the applied drive voltage abnormally. Failure to do so may break ICs. When applying power voltage, check the electrical features beforehand and be careful. Always turn off the power to the LC module controller before removing or inserting the LC module input connector. If the input connector is removed or inserted while the power is turned on, the LC module internal circuit may break.
2) The display response may be late if the operating temperature is under the normal standard, and the display may be out of order if it is above the normal standard. But this is not a failure; this will be restored if it is within the normal standard.
3) The LCD contrast varies depending on the visual angle, ambient temperature, power voltage etc. Obtain the optimum contrast by adjusting the LC dive voltage.
4) When carrying out the test, do not take the module out of the low-temperature space suddenly. Failure to do so will cause the module condensing, leading to malfunctions.
5) Make certain that each signal noise level is within the standard (L level: 0.2Vdd or less and H level: 0.8Vdd or more) even if the module has functioned properly. If it is beyond the standard, the module may often malfunction. In addition, always connect the module when making noise level measurements.
6) The CMOS ICs are incorporated in the module and the pull-up and pull-down function is not adopted for the input so avoid putting the input signal open while the power is ON.
7) The characteristic of the semiconductor element changes when it is exposed to light emissions, therefore ICs on the LCD may malfunction if they receive light emissions. To prevent these malfunctions, design and assemble ICs so that they are shielded from light emissions.

8) Crosstalk occurs because of characteristics of the LCD. In general, crosstalk occurs when the regularized display is maintained. Also, crosstalk is affected by the LC drive voltage. Design the contents of the display, considering crosstalk.

11-5 Other

1) Do not disassemble or take the LC module into pieces. The LC modules once disassembled or taken into pieces are not the guarantee articles.
2) Do not keep the LCD at the same display pattern continually. The residual image will happen and it will damage the LCD. Please use screen saver.
3) AMIPRE will provide one years warrantee for all products and three months warrantee for all repairing products.

12. MECHANICAL DRAWING



1	ENABLE	27	PD15(R3)
2	DOTCLK	28	PD16(R4)
3	HSYNC	29	PD17(R5)
4	VSYNC	30	VDD
5	/CS	31	VCI
6	WR/SCL	32	VCI
7	SDI	33	NC.
8	RS	34	NC.
9	NC	35	NC.
10	/RD	36	NC.
11	/RESRT	37	NC.
12	PD0(B0)	38	NC.
13	PD1(B1)	39	NC.
14	PD2(B2)	40	GND
15	PD3(B3)	41	NC.
16	PD4(B4)	42	NC.
17	PD5(B5)	43	NC.
18	PD6(G0)	44	NC.
19	PD7(G1)	45	GND
20	PD8(G2)	46	SDO
21	PD9(G3)	47	NC.
22	PD10(G4)	48	NC.
23	PD11(G5)	49	NC.
24	PD12(R0)	50	GND
25	PD13(R1)	51	GND
26	PD14(R2)		

Note:
1. Unless indicated, Tolerance ±0.3 is adopted.
2. UV Glue For OLB Protection.
3. Mating Connector:FH26-51S-0.3SHW(HRS).